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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,154	09/21/2001	Harald Boehm	DE920000077US1	4262

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	5

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/960,154	Applicant(s) BOEHM ET AL.	
	Examiner Scott T Baderman	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 11 recites the limitation "the different systems" in line 3. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 12 recites the limitation "the microcode procedures" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 and 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (IEEE).

As in claims 1 and 16, Chang discloses a computer-implemented method for verifying the correctness of the system behavior of a processor cooperating with software that comprises testing the software by using a functional simulator performing in the same way as the hardware of the processor according to the processor's functional specification (pp. 181 and 183: right column), and testing microcode using a hardware emulator behaving in the same way as the hardware of the processor according to the design of the processor's logic gates (pp. 181 and 183: right column).

As in claim 2, Chang discloses a method for verifying the correctness of the system behavior of a CPU comprising a processor hardware and having at least a part of its instructions implemented in microcode (p. 183: right column).

As in claim 3, Chang discloses wherein the microcode includes millicode procedures (which are inherently part of the microcode based on the definition of millicode by the instant application – "most of the instructions running exclusively within the CPU" (see p. 7 of the specification)) and processor code functions (e.g., for booting the computer) (pp. 183: right column and 184: left column), wherein the millicode is tested by using a simulator performing in the same way as the hardware of the processor according to the processor's functional specification (i.e., testing the microcode inherently is testing the millicode as well) (pp. 181 and 183: right column), and a virtual machine (architecture definition) providing a platform for testing the processor code functions (page 183: Figure 6).

As in claim 4, Chang discloses testing microcode (which inherently tests millicode) using a hardware emulator behaving in the same way as the hardware of the processor according to the design of the processor's logic gates (pp. 181 and 183: right column).

As in claim 5, Chang discloses a virtual machine (architecture definition) providing a platform for testing the processor code functions (page 183: Figure 6).

As in claim 6, Chang discloses a simulator interpreting processor code instructions which are not provided by the virtual machine (i.e., when the HDL simulation takes place on the SPARC machine (pp. 183: right column and 184: left column).

As in claim 7, Chang discloses wherein the processor is in communication with a service element code, wherein the service element code is tested independently (i.e., the verification of the OS booting test) (p. 184: left column). The service element code is interpreted as the code used to start the boot process described in Chang (p. 184: left column), which is consistent with the Applicant's specification (see p. 8 of the specification).

As in claim 8, Chang discloses wherein testing the service element code includes disconnecting a service element on which the service element is executed from the processor and providing simulation routines behaving like an attached processor according to its functional specification (pp. 183: right column and 184: left column).

As in claim 9, Chang discloses testing different kinds of microcode (e.g., millicode, etc.) in an environment in which all of the microcodes interact as they would run on the processor (pp. 183: right column and 184: left column).

As in claim 10, Chang discloses wherein testing the different kinds of microcode comprises the step of communicating with a service element code (e.g., when performing the OS boot test) (pp. 183: right column and 184: left column).

As in claim 12, Chang discloses whereby testing the different kinds of microcode includes the step of specifying particular processor code instructions that are not executed by the virtual machine, but by using the microcode procedures instead (i.e., when the HDL-based simulation is being processed on the machines (e.g., SPARC), there are a number of instructions that are not run by the virtual machine) (p. 183: right column).

As in claim 13, Chang discloses testing the microcode by running it on the processor (pp. 183: right column and 184: left column).

As in claim 14, Chang discloses testing the service code element by letting it communicate with the processor (pp. 183: right column and 184: left column).

As in claim 15, Chang discloses wherein testing the software includes the step of providing a high-level description of the processor's functional behavior in a hardware

description language, such as VHDL (pp. 181: left column, 183: right column and 184: left column).

As in claim 17, Chang discloses a system for verifying the correctness of the functional behavior of a processor having at least a part of its instruction set implemented with microcode, wherein the microcode includes millicode procedures (which are inherently part of the microcode based on the definition of millicode by the instant application – "most of the instructions running exclusively within the CPU" (see p. 7 of the specification)) and processor code functions (e.g., for booting the computer) (pp. 183: right column and 184: left column), that comprises a simulator performing in the same way as the hardware of the processor according to the processor's functional specification for testing the millicode (i.e., testing the microcode inherently is testing the millicode as well) (pp. 181 and 183: right column), a virtual machine (architecture definition) providing a platform for testing the processor code functions (page 183: Figure 6) and a hardware emulator behaving in the same way as the hardware of the processor according to the design of the processor's logic gates for testing the microcode (pp. 181 and 183: right column).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (IEEE).

As in claim 11, Chang discloses the method above. However, Chang does not specifically disclose a step of providing a TCP/IP connection between the different systems executing the different kinds of microcodes.

It would have been obvious to a person skilled in the art at the time the invention was made to include a step of providing a TCP/IP connection between the different systems executing the different kinds of microcodes into the method taught by Chang above. This would have been obvious because Chang clearly teaches of a HDL-based verification methodology that can be used for "real-world" application programs (p. 184: right column). A person skilled in the art would have understood that a majority of the "real-world" application programs today include communications over the TCP/IP protocol and would have been motivated to implement the method taught by Chang above into an environment that included a TCP/IP protocol.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB